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10/761,753	01/20/2004	Karl Edwards	LT-106 Div . 2	2868

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EXAMINER	
NGUYEN, HIEP	
ART UNIT	**PAPER NUMBER**
2816	

DATE MAILED: 02/01/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/761,753	EDWARDS, KARL	
	Examiner	Art Unit	
	Hiep Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 November 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5-24,38 and 39* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5-24,38 and 39* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Correction and/or clarification is required.

Regarding claims 1 and 5, the recitation " wherein the first trigger signal creates a very small difference in voltage at the SET transistor" on lines 15-16 of claim 1 and on lines 19-20 of claim 5 is indefinite because. In the Remarks, the Applicant admits that the circuit of claims 1 and 5 read on figure 2 of the present application. According to figure 2, the SET and RESET signals are applied directly to the bases of the SET and RESET transistors (110, 140). Therefore, the bases of the SET and RESET transistors receive the voltages that are applied to them from the external circuit. These (trigger) signals are not necessary to be very small as recited. It is also not clear what the "very small difference in voltage" is meant by. As understood by the examiner, the "very small difference in voltage" is the voltage applied to base of the SET or RESET transistor that is not necessary to be small. If the SET /RESET transistors are not low threshold transistors, the input signals applied to the SET/RESET transistors will not "create a very small difference in voltage" as recited. However, if the SET and RESET transistors are low threshold bipolar transistors (USP. 5,541,456), low trigger voltages can be used to turn the SET and RESET transistors on. The same rationale is applied to the recitation " wherein the first trigger signal creates a very small difference in voltage at the RESET transistor" on lines 19-21 of claim 1 and lines 23-24 of claim 5.

Regarding claim 3, the recitation "level-shifting circuit" is indefinite because it is misdescriptive. No such circuit is seen in figure 2 of the present application.

Claim 6 is indefinite because it is misdescriptive. No "temperature compensating the oscillator" is seen in figure 2.

Regarding claims 7, 8 and 10-12, the recitations " an oscillator capacitor coupled to the SET circuit" in claim 7, "the capacitor" in claim 8 and " oscillator transistor" in claims 10-12 are indefinite because they are misdescriptive. Claims 7 and 10-12 depend upon claim 1. Claim 1 reads on figure 2 and figure 2 does not show the "oscillator capacitor" and the "oscillator transistor".

Regarding claims 13 and 14, the recitation " a de-bias circuit" is indefinite because it is misdescriptive. The "de-bias circuit" is not shown in figure 2.

Regarding claim 19, the recitation "the total current is substantially continuously conducted by the SET circuit" is indefinite because it is misdescriptive. In figure 2, two transistors of the SET circuit (225) are not turned on at the same time thus; the total current is not continuously conducted by the SET circuit.

Regarding claim 20, the recitation "the total current is substantially continuously conducted by the RESET circuit" is indefinite because it is misdescriptive. In figure 2, two transistors of the RESET circuit (245) are not turned on at the same time thus; the total current is not continuously conducted by the SET circuit.

Regarding claims 21 and 22, the recitation " when said first trigger signal is applied to said SET circuit, said RESET circuit switches ON" is indefinite because it is misdescriptive. Figure 2 shows that when a trigger signal is applied to input (190) of the SET circuit, the SET circuit is switched on and the RESET circuit (245) is not switched on as recited.

Claims 23 and 24 are indefinite because they are misdescriptive. Figure 2 shows that the voltage applied to the gates of the SET/RESET transistors must be higher than 0.018 volts unless these transistors are native transistors.

Regarding claims 38 and 39, the recitation "wherein the first trigger signal is less than the full Vbe voltage of the SET transistor" is indefinite because it is misdescriptive. Figure 2 shows that the SET and RESET transistors having bases connected directly to input trigger signals thus, the input trigger signals must have magnitudes higher than the full Vbe voltages of the SET and RESET transistors to turn them on.

Claims 2, 15-18 are indefinite because of the technical deficiencies of claims 1 and 5.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-3, 5, 6, 38 and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nolan et al. (US Pat. 6,020,792) in view of Maggioni et al. (US Pat. 5,541,456).

Regarding claims 1-3, figure 3 of Nolan shows a latch circuit having an output (166), the output having a first state and a second state, the output being controllable by a first trigger signal (162) and second trigger signal (164), the latch circuit comprising:

a SET circuit, not shown, having an input connected to the (S) input;

a RESET circuit not shown, having an input connected to the (R) input.

The SET/RESET flip-flop circuit has the following basic function (see attached US Pat. 5,541,544): when a first trigger signal applied to the (S) input reaches a first threshold, a current is conducted by the SET circuit and the SET output (Q) is high. When a second trigger signal applied to the (R) input reaches a second threshold, a current conducted by the RESET circuit and the RESET output (QN) is high. Figure 3 of Nolan does not show that the first and second trigger signals have very low threshold voltage at the SET circuit. Figure 1 of Maggioni teaches a low threshold bipolar transistor having low threshold voltage for ensuring fast switching function (Abstract, col. 4, lines 12-20). Therefore, it would have been obvious to an artisan having skills in the art to replace the input transistors of the SET/RESET circuit of Nolan with the low threshold transistors taught by Maggioni for providing fast latch circuit. Figure 3 of Nolan shows that the latch circuit forms a switching portion of an oscillator circuit. Figure 3 is a circuit of a temperature-compensated oscillator circuit (Abstract and col.3, lines 55-66). The level-shifting circuit is circuit 150.

Regarding claims 5, 6, 38 and 39, figure 3 of Nolan shows a method oscillating the output an oscillator, the output having a first state and a second state, the oscillator including a latch (160), the latch including a first latch transistor a second latch transistor, a SET

transistor and a RESET transistor (well known, not shown including in circuit 160), the method comprising:

at the first state, conducting a first current in the first latch transistor and the SET transistor such that the SET transistor is biased at a point close first threshold by the SET input signal);

at the second state, conducting the first current in the second latch transistor and the RESET transistor such that the RESET transistor is biased at a point close to a second threshold (by the RESET input signal);

varying the output from the first state to the second state by providing a trigger current raise the base of the SET transistor over a first threshold; and varying the output from the second state to the first state by providing the trigger current to raise the base of the RESET transistor over second threshold. Figure 3 of Nolan does not show that the first and second trigger signals have low threshold voltage at the SET/RESET circuits. Figure 1 of Maggioni teaches a low threshold bipolar transistor having low threshold voltage for ensuring fast switching function (Abstract, col. 4, lines 12-20). Therefore, it would have been obvious to an artisan having skills in the art to replace the input transistors of the set/reset circuit with the low threshold transistors taught by Maggioni for providing fast latch circuit. Note that the above method of functioning a SET/RESET flip-flop is basically well known (see reference 5,541,544). By applying a signal to SET/RESET inputs of the SET-RESET flip-flop, the outputs of the flip-flop change states when the input signals of the flip-flop circuit reach the thresholds of the SET/RESET transistors. Figure 3 of Nolan shows a temperature-compensating oscillator. With the transistors of Maggioni the threshold voltage is less that the normal Vbe voltage of the regular bipolar transistors.

Claims 1, 15-17, 19-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakano (US Pat. 5,541,544) in view of Maggioni et al. (US Pat. 5,541,456).

Regarding claims 1, 15-17, 19-24, figure 6 of Nakano shows a latch having a SET circuit and a RESET circuit. Figure 6 of Nakano does not show that the first and second trigger signals have very low threshold voltage at the SET circuit. Figure 1 of Maggioni teaches a low threshold bipolar transistor having low threshold voltage for ensuring fast

switching function (Abstract, col. 4, lines 12-20). Therefore, it would have been obvious to an artisan having skills in the art to replace the input transistors of the set/reset circuit of Nakano with the low threshold transistors taught by Maggioni for providing fast latch circuit. The current sources are current sources (I3) and (I6). When the SET/RESET circuit is turned on, they conduct the total current. With low threshold transistor, the trigger voltage can be very low such as 0.018 volts.

Regarding claim 18, the combination of Nakano and Maggioni includes all the limitations of claim 18 except for the limitation that the total current is about 200 microamperes. However, it is old and well known and it would have been an obvious matter of preference bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose the particular claimed relative predetermined value of a differential input voltage limitations because applicant has not disclosed that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical, and it appears prima facie that the process would possess utility using another relative predetermined value of a differential input voltage. Indeed, it has been held that optimization of range limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See MPEP 2144.05(II): "Generally, differences in concentration or temperature will not support the patentability of subject matter encompassed by the prior art unless there is evidence indicating such concentration or temperature is critical. '[W]here the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation.'" In re Aller, 220 F.2d 454, 105 USPQ 233, 235 (CCPA 1955). See also In re Hoeschele, 406 F.2d 1403, 160 USPQ 809 (CCPA 1969), Merck & Co. Inc. v. Biocraft Laboratories Inc., 874 F.2d 804, 10 USPQ2d 1843 (Fed. Cir.), cert. denied, 493 U.S. 975 (1989), and In re Kulling, 897 F.2d 1147, 14 USPQ2d 1056 (Fed. Cir. 1990). As set forth in MPEP 2144.05(III). Therefore, it would have been obvious to one having ordinary skill in the art to select the low threshold transistors so that the latch circuit can function with a very low current of about 200 microamperes dependent upon particular environment of use to ensure optimum performance.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hiep Nguyen whose telephone number is (571) 272-1752. The examiner can normally be reached on Monday to Friday from 7:30am to 4:00pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

01-30-06

TUAN T. LAM
PRIMARY EXAMINER